Group Number and Name	**Dec14-12**
Client/Advisor	**Bong Wie**
Attendees/Role	**Sean Nichols/Leader, Chi Hoe How/Communication, Yishu Mei/Webmaster/ Meng Lu/Advisor**

Past Week Accomplishments

- **Yishu** - Got a stepper motor to rotate smoothly. The group worked together to work out the rest of the kinks of this test code.

- **Sean** - K-means hardware core fully assembled and tested via simulation!

- **Chi Hoe -** Merge previous presentation to Prezi.

- **Sean** - Implemented testbench module that is an abstraction of the AXI4-Stream protocol. The testbench takes in a 24 bit color depth bitmap file and stimulates an AXI4-Stream bus. Will prove handy when running final simulations

Plan for Coming Week

- **Yishu** - Implement use of CTC hardware on ATMega 328 to control the steps of the stepper motor. This will reduce processing overhead with manually flipping bits.

- **Yishu** - Implement acceleration calculation as function call back from timer interrupt.

- **Sean Nichols** - Continue to construct hardware modules for the AXI4-Stream interface to the K-means core. Needed : Frame timing module, row/col counter, pixel matching comparator module with register hook, request control module, etc...

- **Sean Nichols** - Come up with final register set for K-means logic core.

- **Sean Nichols** - Run build test on stand alone K-means core to see if it will fit on the Zynq FPGA.

- **Chi Hoe** - Add a clocked process to the AXI4-Stream passthrough module to continue to prove that this will not affect video performance.

- **Chi Hoe** - Merge Xilinx generated “user logic” code to successfully merge in AXI4-Lite register interface into AXI4-Stream module.

Pending Issues

- It has been noted that one stepper motor driver has been burnt out. We must do additional testing to conclude this. If so, we will need to order a new one

- Another issue is that the FPGA we are working with may not be big enough. Please refer to extended conversation below.

Individual Hourly Contributions

Name	**Hours this week**	**Hours Cumulative**
Sean Nichols	20	128
Chi Hoe How	18	88
Yishu Mei	20	87

Comments and Extended Discussions

- If the design will not fit on the Zynq FPGA, then this will be a MAJOR drawback. We will need to reconsider what logic to trim based on the specific problem. So far it appears that this could arise from two sources
    - 1) The amount of Block RAM resources available after the existing pipeline.
    - 2) The amount of logic required for tracking 16 objects simultaneously in hardware is great.
        - There simply may not be enough LUTs on the FPGA to fully implement our design
        - Routing Congestion…
    - 3) Timing may become an issue for LARGE combinatorial paths when constrained to 145MHz. We may have to look into a bit of pipelining control to fix this.